FIG. 1

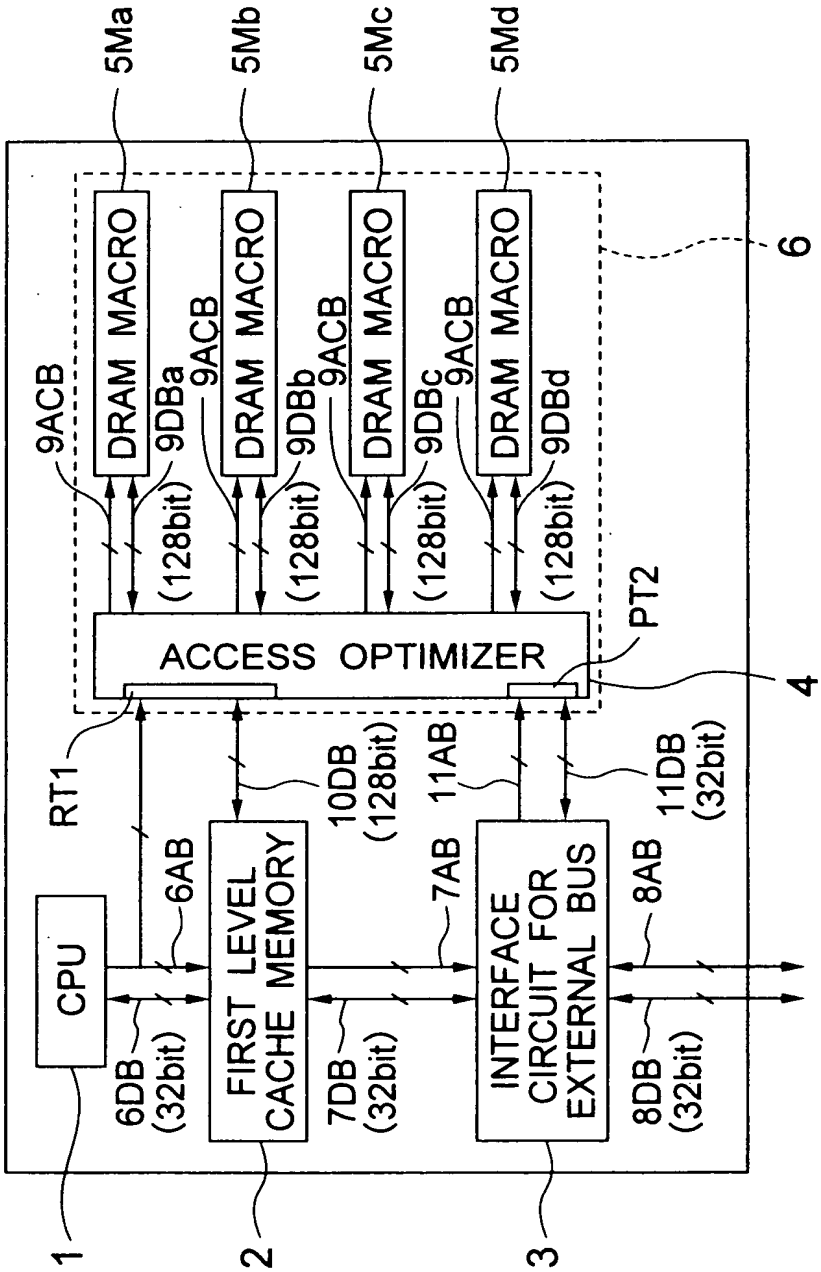

5Ma
5Mb
5Mc
5Md
DRAM MACRO
DRAM MACRO
DRAM MACRO
DRAM MACRO
6
9ACB
9DBa
9ACB
9DBb
9ACB
9DBc
9ACB
9DBd
(128bit)
(128bit)
(128bit)
(128bit)
ACCESS OPTIMIZER
PT2
4
RT1
10DB
(128bit)
11AB
11DB
(32bit)
CPU
6AB
FIRST LEVEL
CACHE MEMORY
7AB
INTERFACE
CIRCUIT FOR
EXTERNAL BUS
8AB
6DB
(32bit)
7DB
(32bit)
8DB
(32bit)
1
2
3

FIG. 2

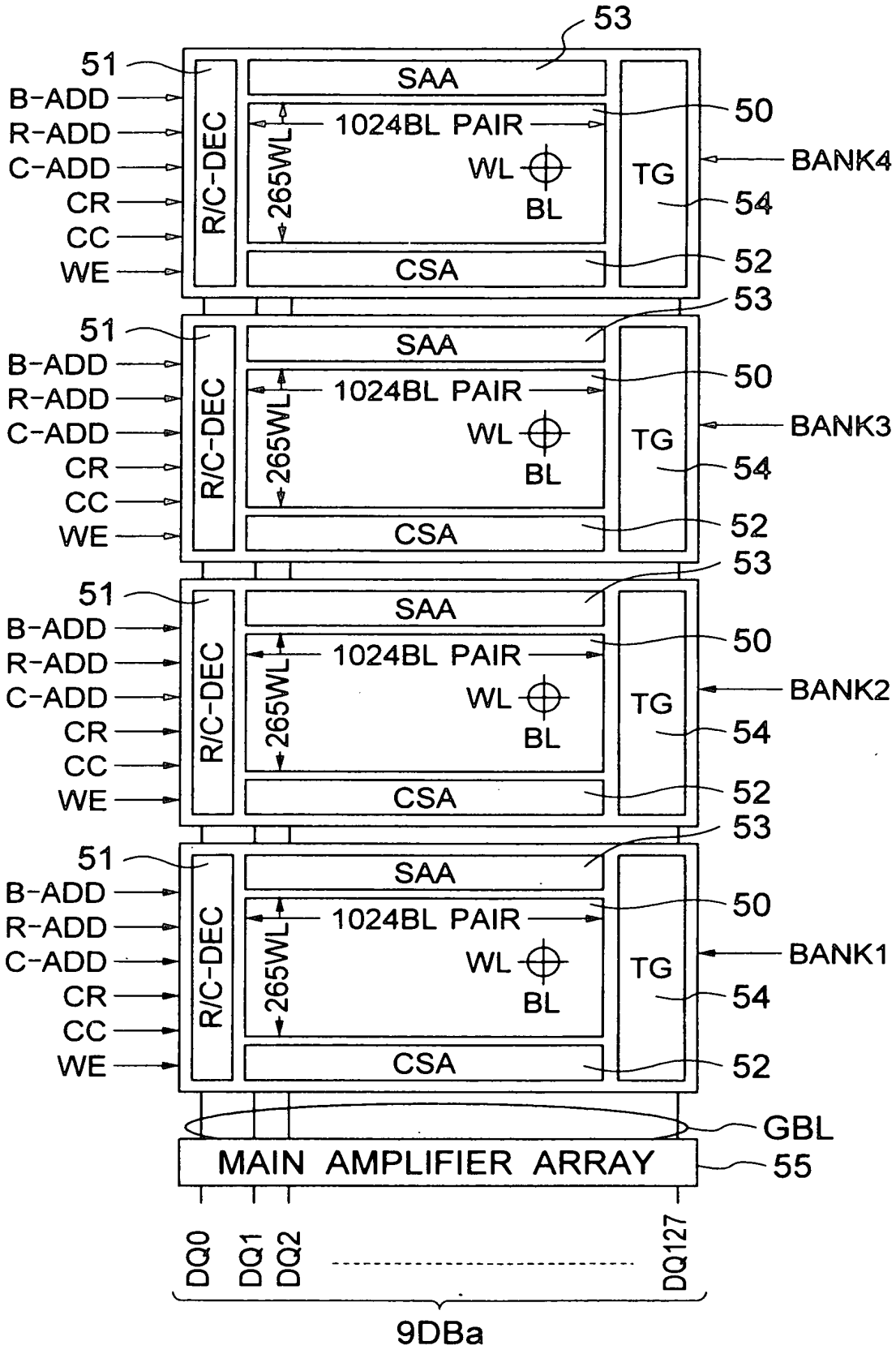

53
51
B-ADD
R-ADD
C-ADD
CR
CC
WE
R/C-DEC
SAA
1024BL PAIR
265WL
WL
BL
TG
50
54
52
CSA
BANK4
BANK3
BANK2
BANK1
GBL
MAIN AMPLIFIER ARRAY
55
DQ0
DQ1
DQ2
DQ127
9DBa

FIG. 3

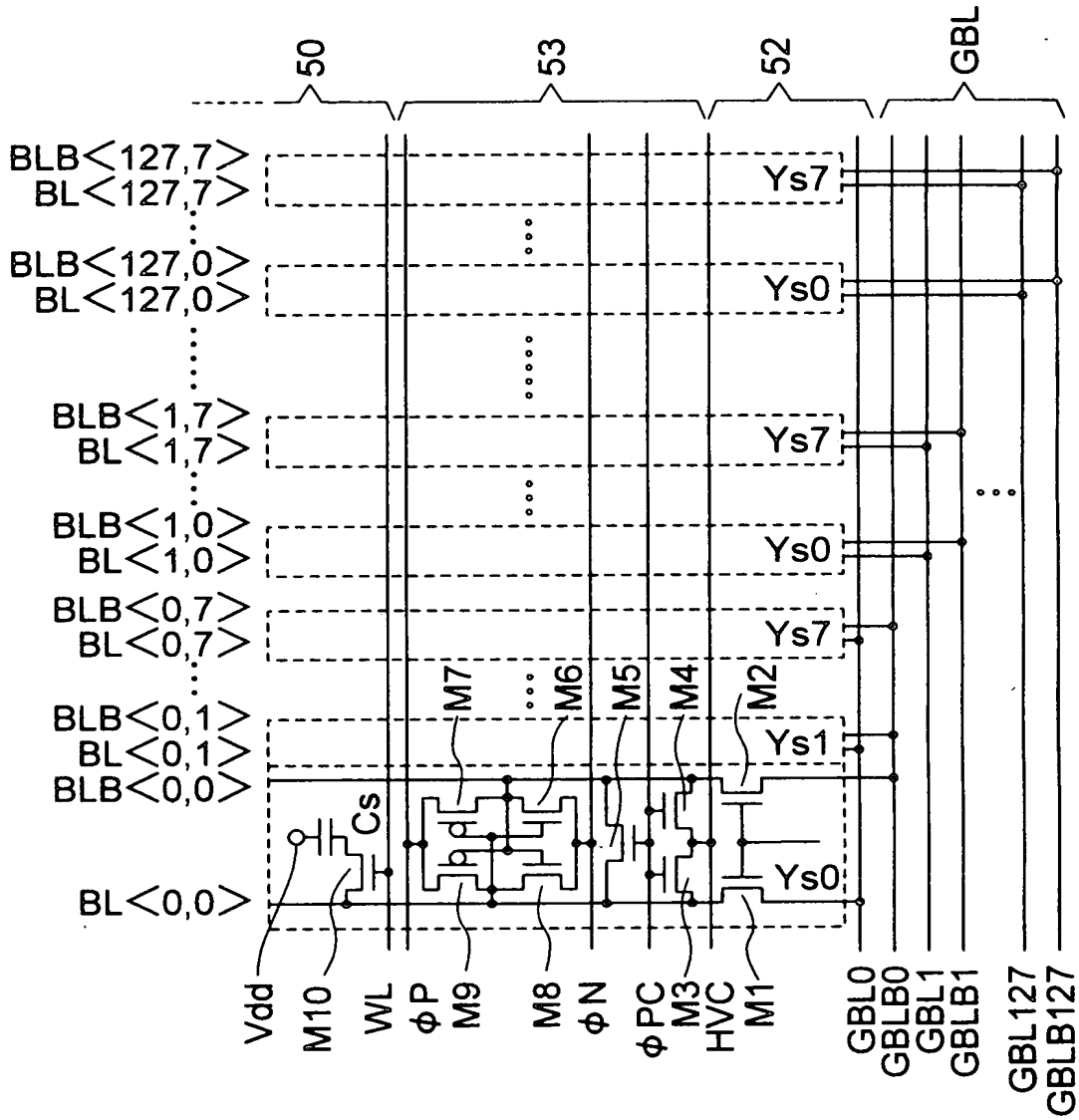

50
53
52
GBL
BLB<127,7>
BL<127,7>
BLB<127,0>
BL<127,0>
BLB<1,7>
BL<1,7>
BLB<1,0>
BL<1,0>
BLB<0,7>
BL<0,7>
BLB<0,1>
BL<0,1>
BLB<0,0>
BL<0,0>
Ys7
Ys0
Ys7
Ys0
Ys7
Ys1
Ys0
Cs
M7
M6
M5
M4
M2
Vdd
M10
WL
φP
M9
M8
φN
φPC
M3
HVC
M1
GBL0
GBLB0
GBL1
GBLB1
GBL127
GBLB127

FIG. 4

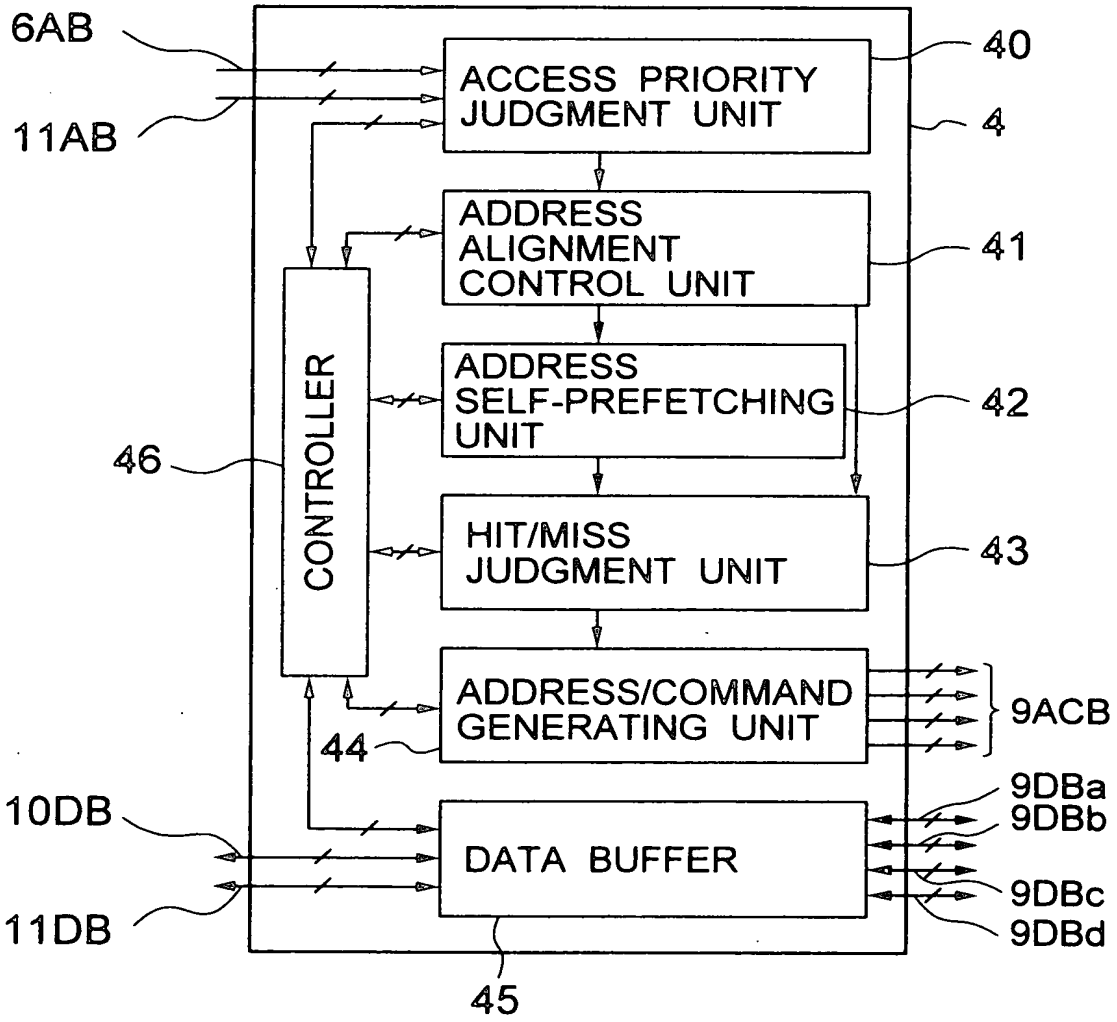

6AB
11AB
ACCESS PRIORITY JUDGMENT UNIT
40
4
ADDRESS ALIGNMENT CONTROL UNIT
41
CONTROLLER
ADDRESS SELF-PREFETCHING UNIT
42
46
HIT/MISS JUDGMENT UNIT
43
ADDRESS/COMMAND GENERATING UNIT
9ACB
44
10DB
9DBa
9DBb
DATA BUFFER
9DBc
11DB
9DBd
45

FIG. 5

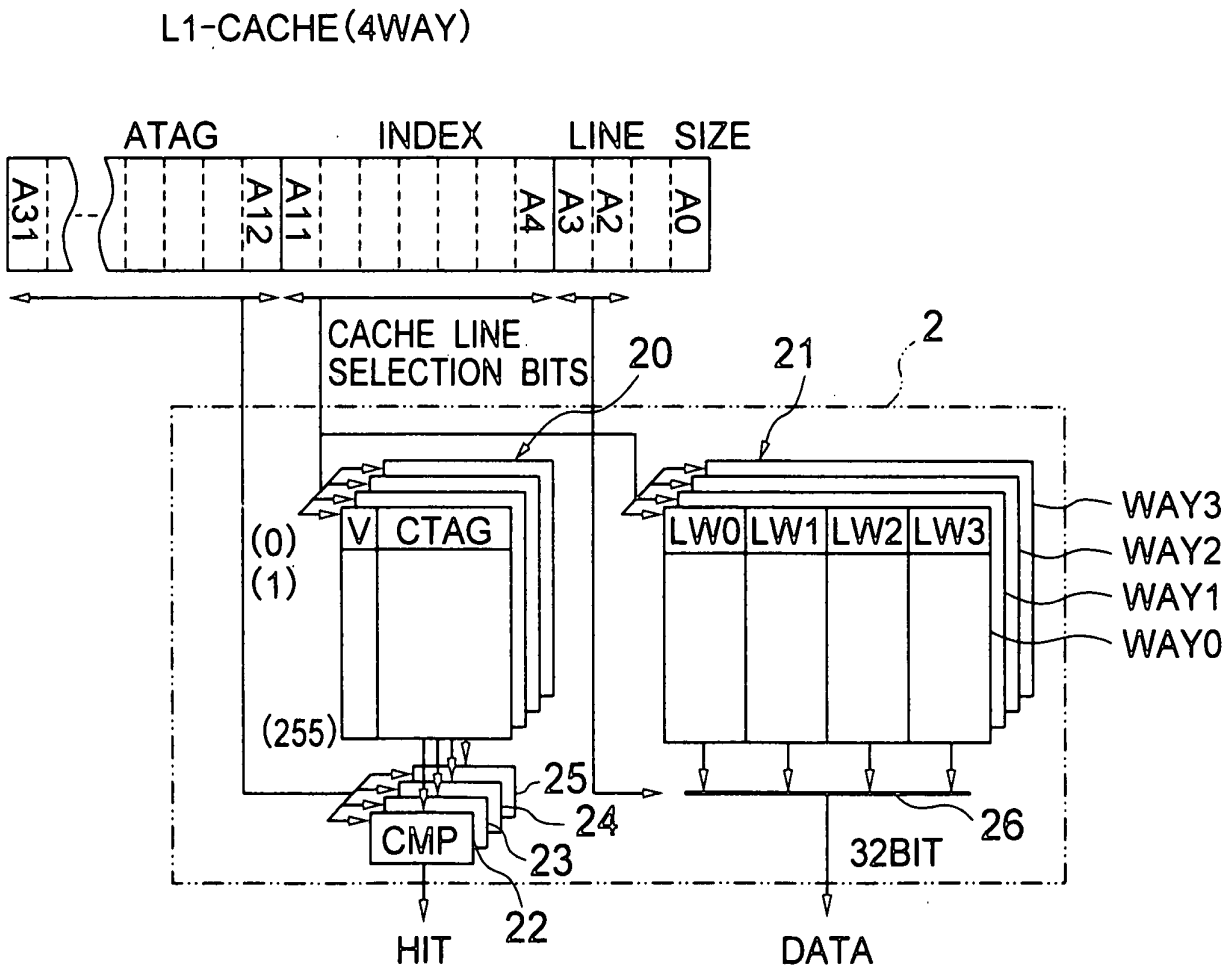

L1-CACHE(4WAY)
ATAG
INDEX
LINE SIZE
A31
A12
A11
A4
A3
A2
A0
CACHE LINE SELECTION BITS
20
21
2
V
CTAG
LW0
LW1
LW2
LW3
WAY3
WAY2
WAY1
WAY0
(0)
(1)
(255)
25
24
23
22
26
CMP
32BIT
HIT
DATA

FIG. 6

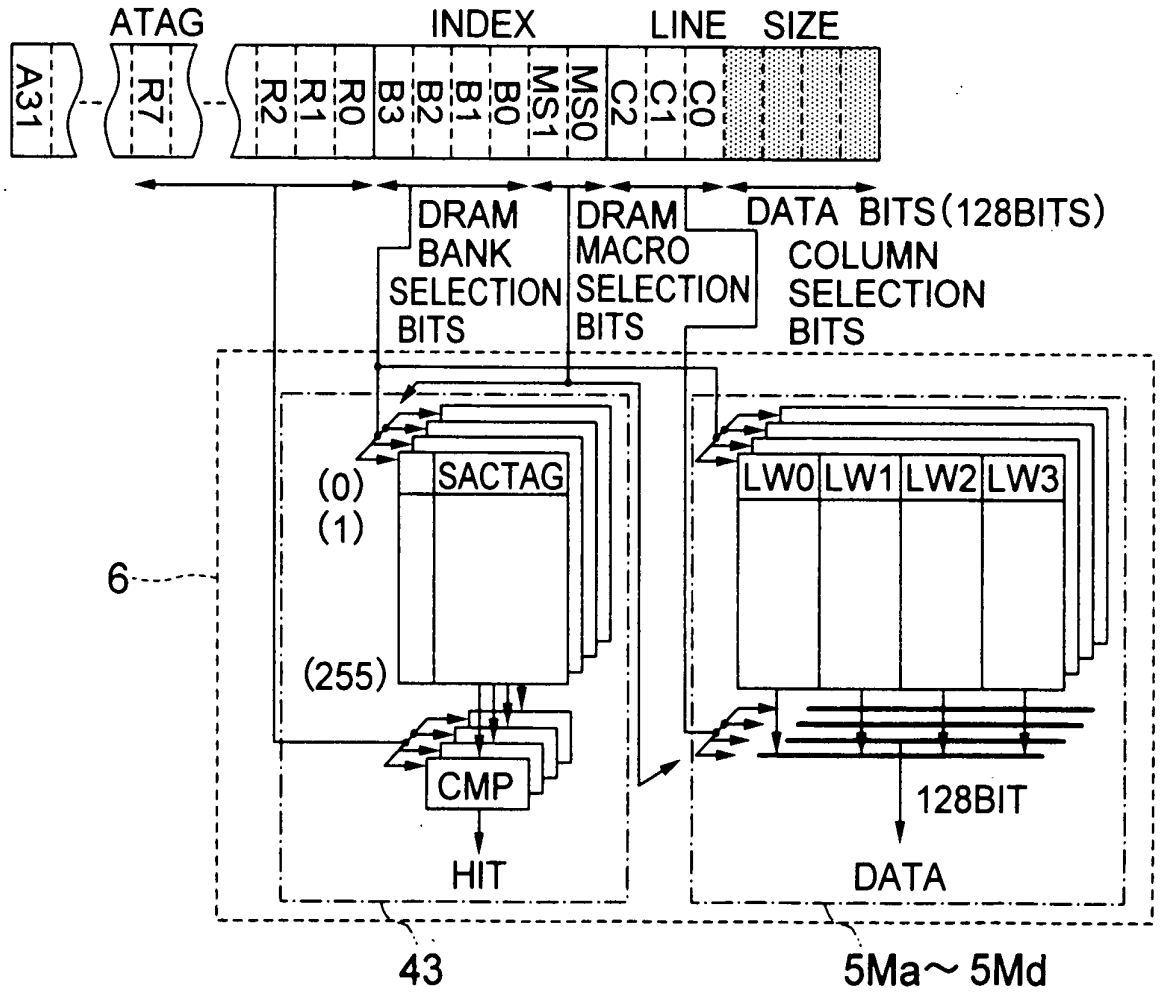

ATAG
INDEX
LINE
SIZE
A31
R7
R2
R1
R0
B3
B2
B1
B0
MS1
MS0
C2
C1
C0
DRAM BANK SELECTION BITS
DRAM MACRO SELECTION BITS
DATA BITS(128BITS) COLUMN SELECTION BITS
(0)
(1)
(255)
SACTAG
LW0
LW1
LW2
LW3
CMP
HIT
128BIT
DATA
6
43
5Ma~ 5Md

FIG. 7

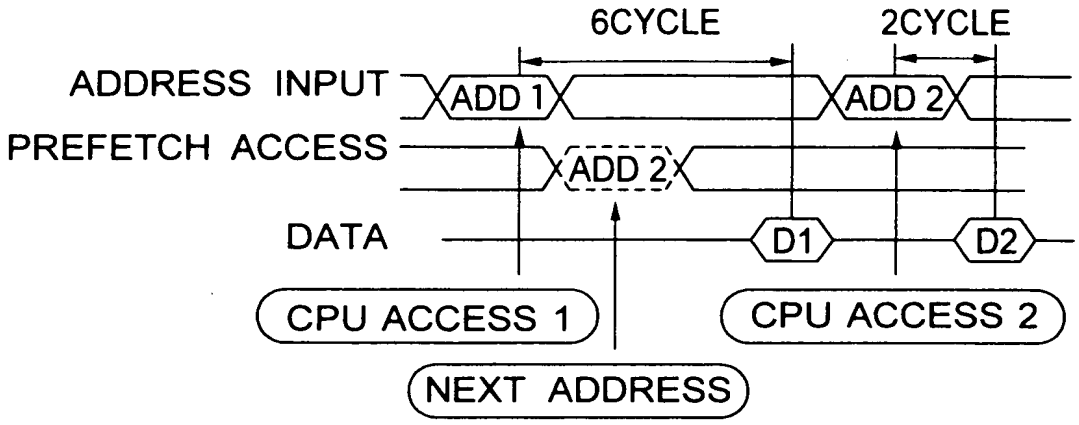

6CYCLE
2CYCLE
ADDRESS INPUT
ADD 1
ADD 2
PREFETCH ACCESS
ADD 2
DATA
D1
D2
CPU ACCESS 1
CPU ACCESS 2
NEXT ADDRESS

FIG. 8

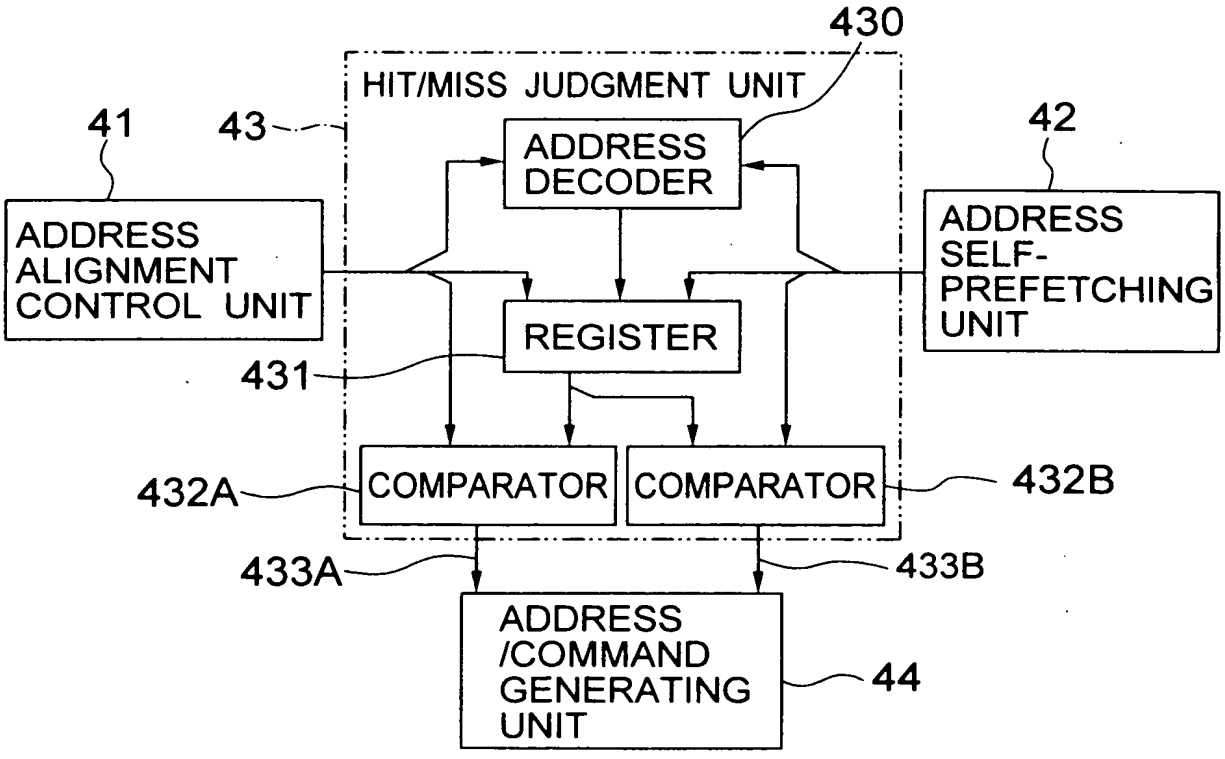

430
HIT/MISS JUDGMENT UNIT
41
43
42
ADDRESS DECODER
ADDRESS ALIGNMENT CONTROL UNIT
ADDRESS SELF-PREFETCHING UNIT
REGISTER
431
COMPARATOR
COMPARATOR
432A
432B
433A
433B
ADDRESS /COMMAND GENERATING UNIT
44

FIG. 9

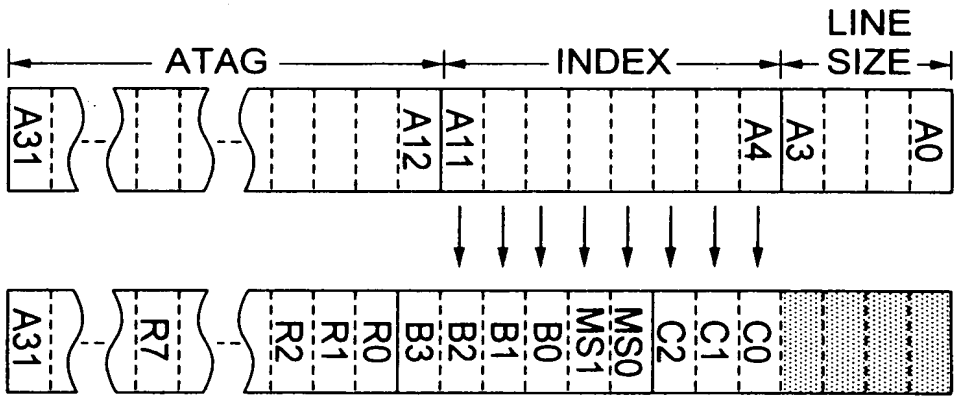

ATAG
INDEX
LINE SIZE
A31
A12
A11
A4
A3
A0
A31
R7
R2
R1
R0
B3
B2
B1
B0
MS1
MS0
C2
C1
C0

FIG. 10

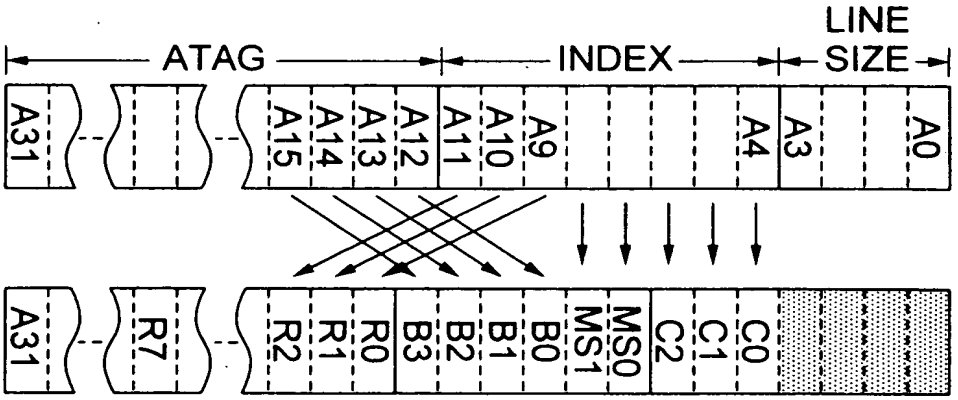

ATAG
INDEX
LINE SIZE
A31
A15
A14
A13
A12
A11
A10
A9
A4
A3
A0
A31
R7
R2
R1
R0
B3
B2
B1
B0
MS1
MS0
C2
C1
C0

FIG. 11

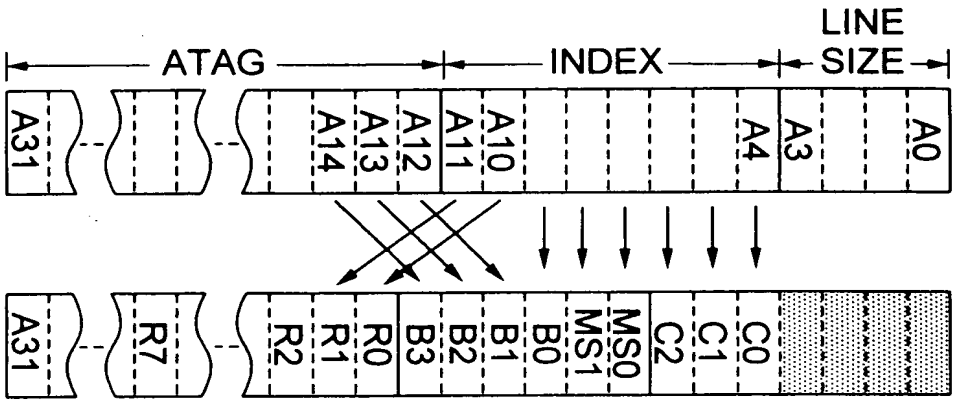

ATAG
INDEX
LINE SIZE
A31
A14
A13
A12
A11
A10
A4
A3
A0
A31
R7
R2
R1
R0
B3
B2
B1
B0
MS1
MS0
C2
C1
C0

FIG. 12

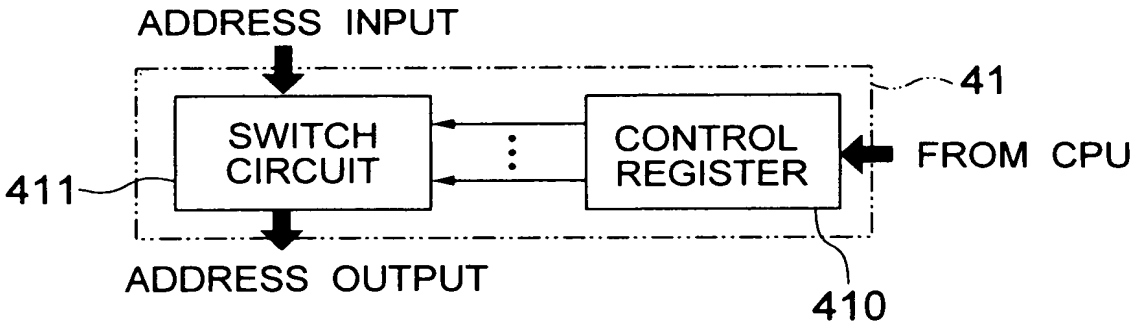

ADDRESS INPUT
41
SWITCH CIRCUIT
CONTROL REGISTER
FROM CPU
411
ADDRESS OUTPUT
410

FIG. 13

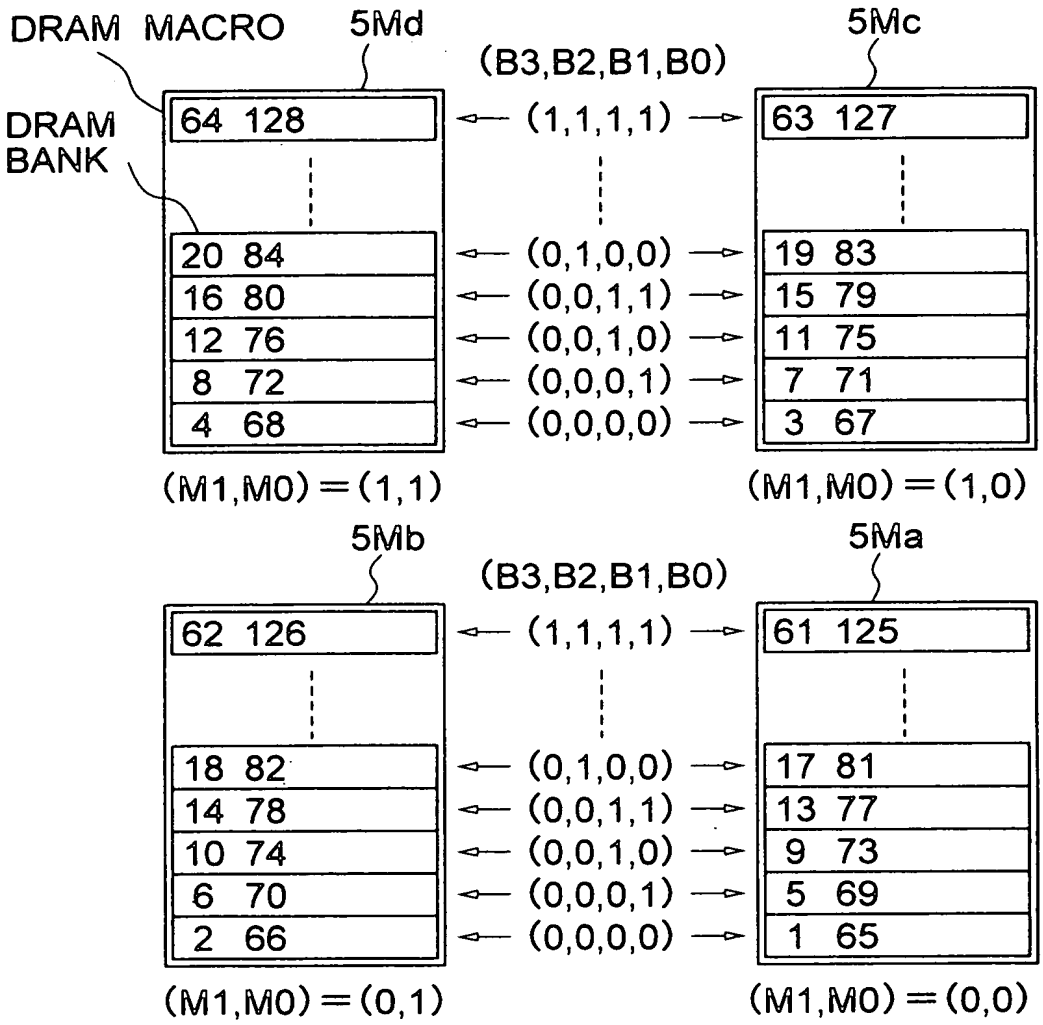

DRAM MACRO
DRAM BANK
5Md
5Mc
5Mb
5Ma
(B3,B2,B1,B0)
64 128
63 127
(1,1,1,1)
20 84
16 80
12 76
8 72
4 68
19 83
15 79
11 75
7 71
3 67
(0,1,0,0)
(0,0,1,1)
(0,0,1,0)
(0,0,0,1)
(0,0,0,0)
(M1,M0)=(1,1)
(M1,M0)=(1,0)
62 126
61 125
18 82
14 78
10 74
6 70
2 66
17 81
13 77
9 73
5 69
1 65
(M1,M0)=(0,1)
(M1,M0)=(0,0)

FIG. 14

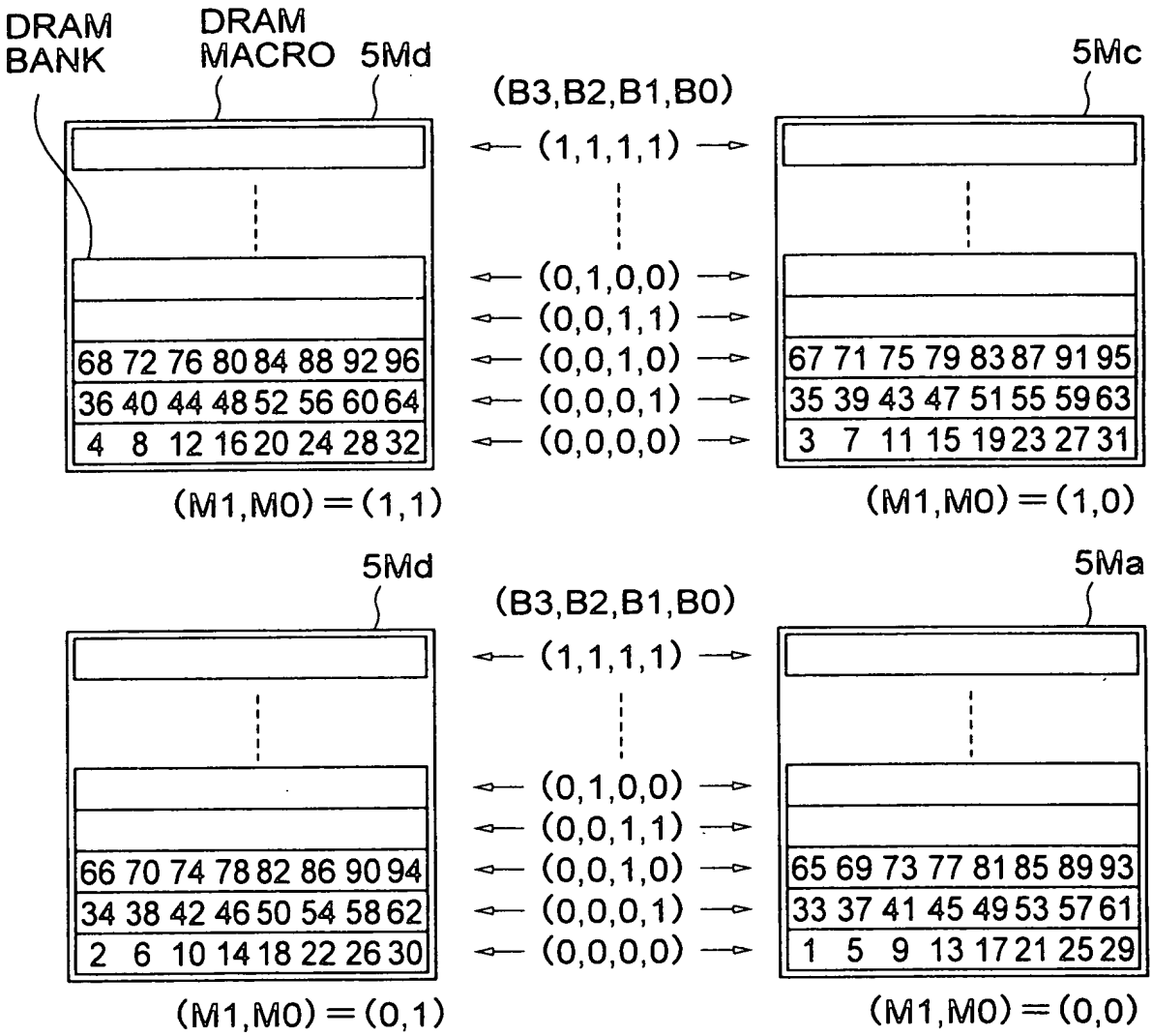

DRAM BANK
DRAM MACRO
5Md
(B3,B2,B1,B0)
(1,1,1,1)
(0,1,0,0)
(0,0,1,1)
(0,0,1,0)
(0,0,0,1)
(0,0,0,0)
5Mc
68 72 76 80 84 88 92 96
36 40 44 48 52 56 60 64
4 8 12 16 20 24 28 32
67 71 75 79 83 87 91 95
35 39 43 47 51 55 59 63
3 7 11 15 19 23 27 31
(M1,M0) = (1,1)
(M1,M0) = (1,0)
5Md
5Ma
(B3,B2,B1,B0)
(1,1,1,1)
(0,1,0,0)
(0,0,1,1)
(0,0,1,0)
(0,0,0,1)
(0,0,0,0)
66 70 74 78 82 86 90 94
34 38 42 46 50 54 58 62
2 6 10 14 18 22 26 30
65 69 73 77 81 85 89 93
33 37 41 45 49 53 57 61
1 5 9 13 17 21 25 29
(M1,M0) = (0,1)
(M1,M0) = (0,0)

FIG. 15

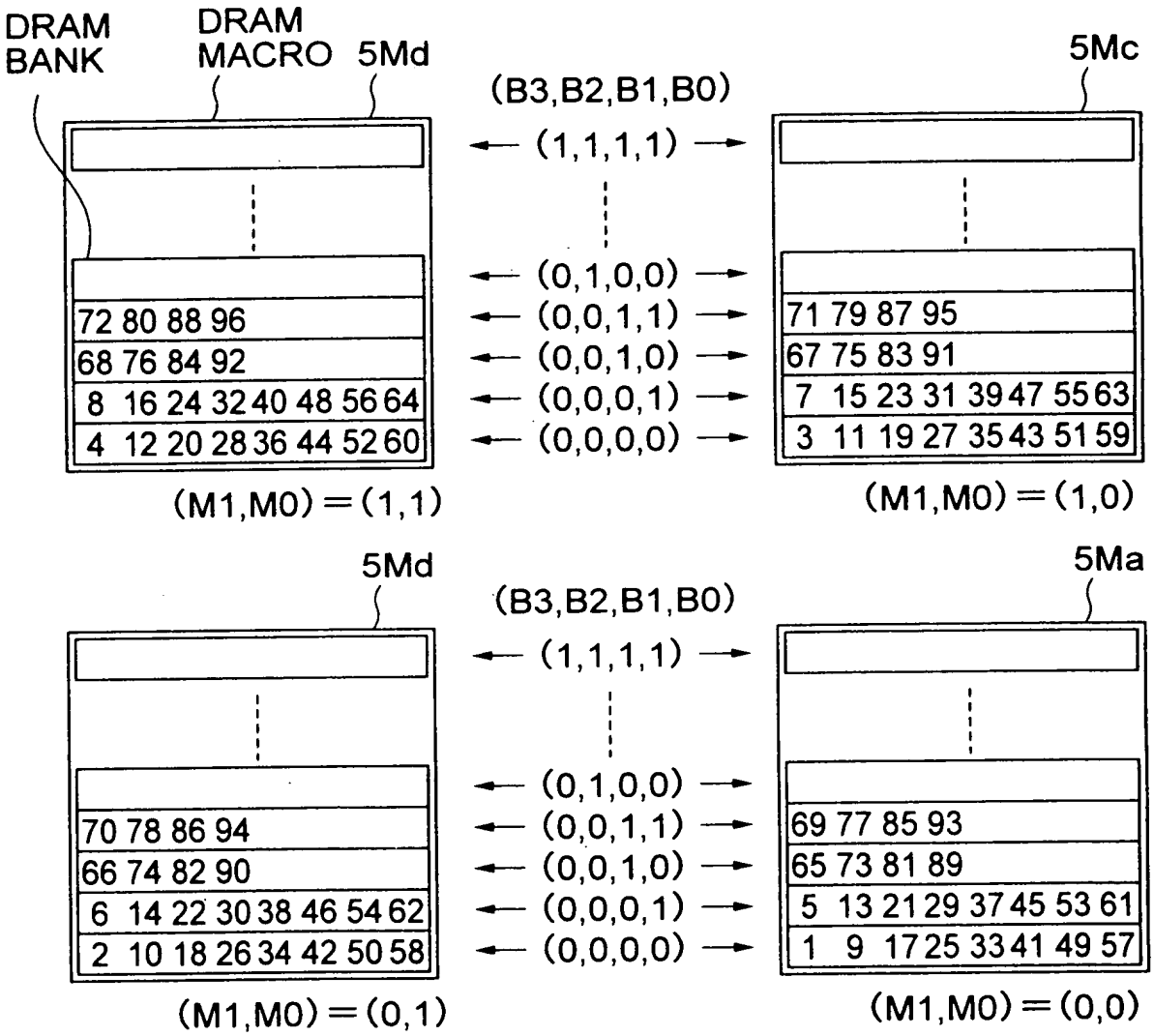

DRAM BANK
DRAM MACRO
5Md
(B3,B2,B1,B0)
5Mc
(1,1,1,1)
(0,1,0,0)
(0,0,1,1)
(0,0,1,0)
(0,0,0,1)
(0,0,0,0)
72 80 88 96
68 76 84 92
8 16 24 32 40 48 56 64
4 12 20 28 36 44 52 60
71 79 87 95
67 75 83 91
7 15 23 31 39 47 55 63
3 11 19 27 35 43 51 59
(M1,M0) = (1,1)
(M1,M0) = (1,0)
5Md
(B3,B2,B1,B0)
5Ma
(1,1,1,1)
(0,1,0,0)
(0,0,1,1)
(0,0,1,0)
(0,0,0,1)
(0,0,0,0)
70 78 86 94
66 74 82 90
6 14 22 30 38 46 54 62
2 10 18 26 34 42 50 58
69 77 85 93
65 73 81 89
5 13 21 29 37 45 53 61
1 9 17 25 33 41 49 57
(M1,M0) = (0,1)
(M1,M0) = (0,0)

FIG. 16

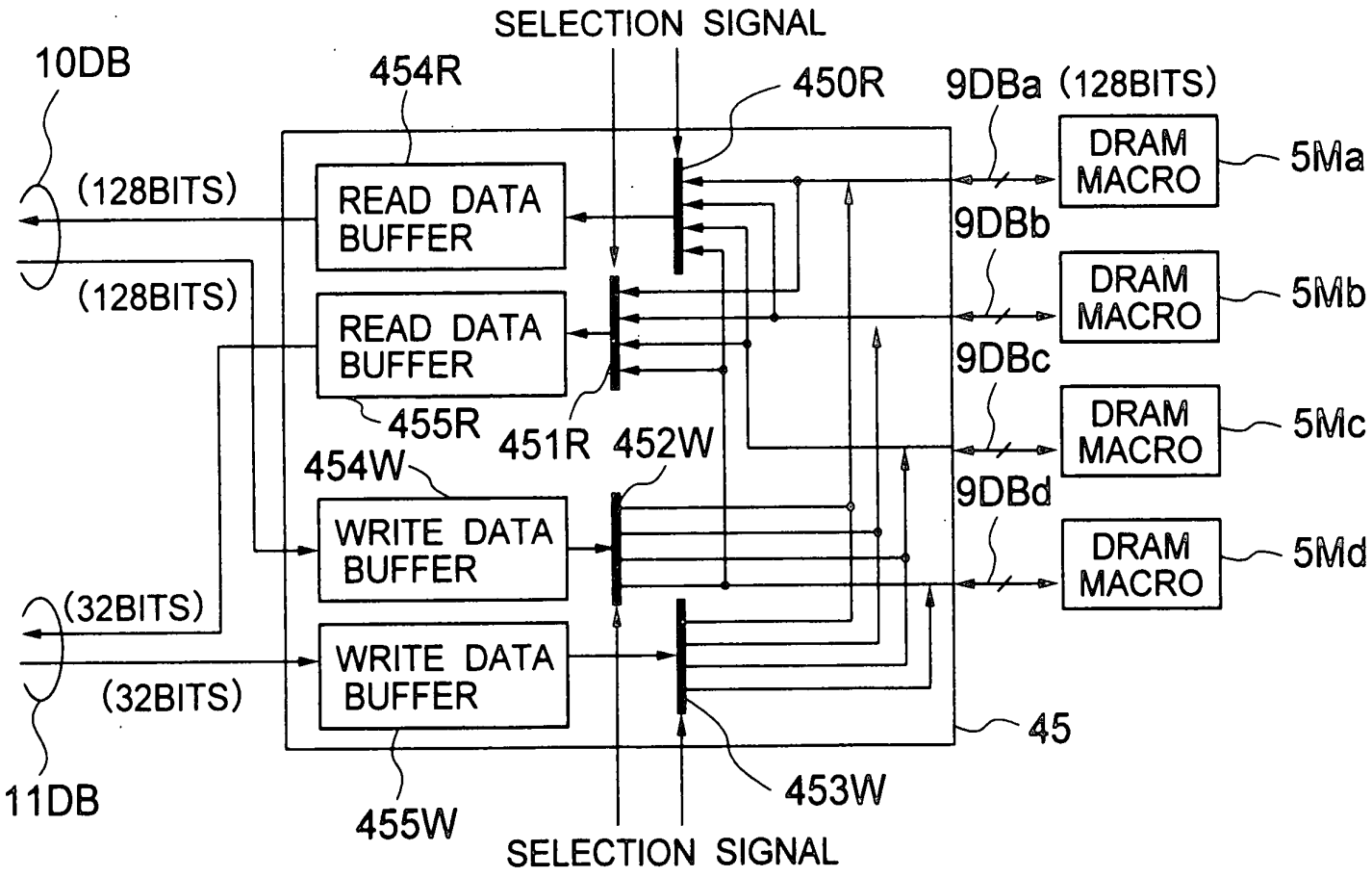

SELECTION SIGNAL
10DB
454R
450R
9DBa (128BITS)
DRAM MACRO
5Ma
(128BITS)
READ DATA BUFFER
9DBb
DRAM MACRO
5Mb
(128BITS)
READ DATA BUFFER
9DBc
DRAM MACRO
5Mc
455R
451R
452W
454W
9DBd
WRITE DATA BUFFER
DRAM MACRO
5Md
(32BITS)
WRITE DATA BUFFER
(32BITS)
45
11DB
455W
453W
SELECTION SIGNAL

FIG. 17

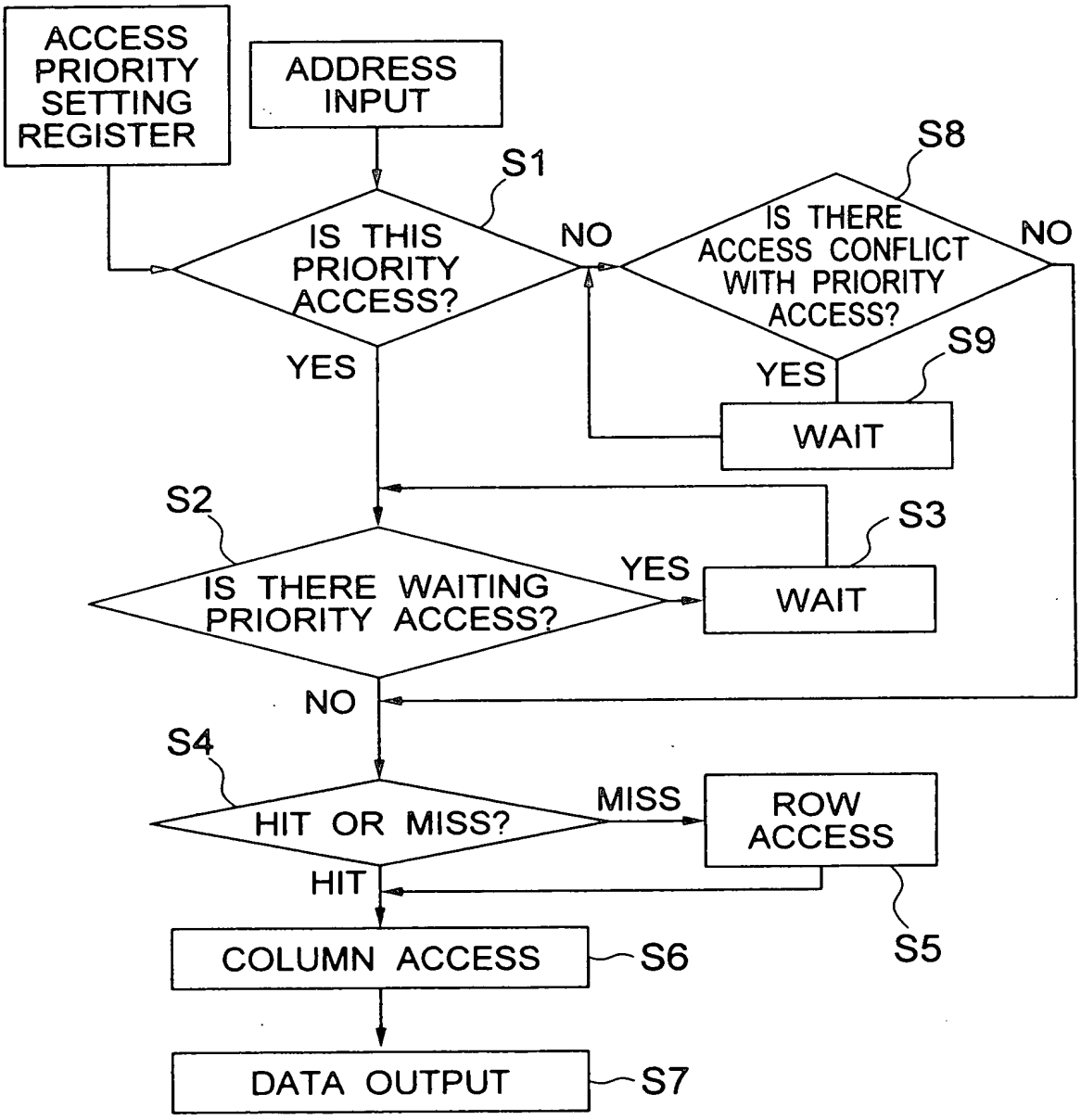

ACCESS PRIORITY SETTING REGISTER
ADDRESS INPUT
S1
IS THIS PRIORITY ACCESS?
NO
YES
S8
IS THERE ACCESS CONFLICT WITH PRIORITY ACCESS?
NO
YES
S9
WAIT
S2
IS THERE WAITING PRIORITY ACCESS?
YES
S3
WAIT
NO
S4
HIT OR MISS?
MISS
ROW ACCESS
S5
HIT
COLUMN ACCESS
S6
DATA OUTPUT
S7

FIG. 18A

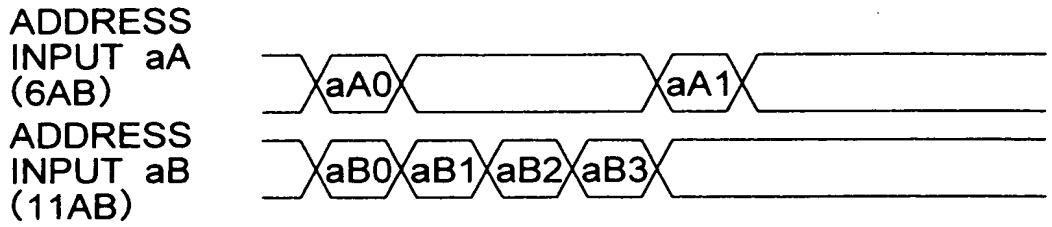


FIG. 18B

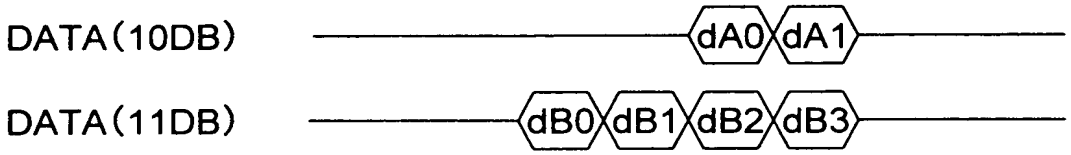


FIG. 18C

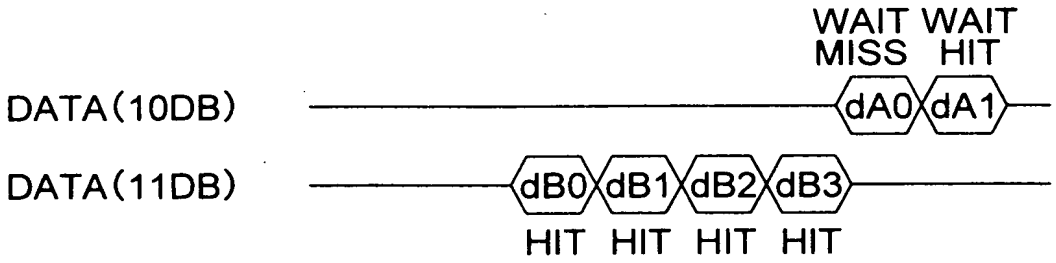


FIG. 18D

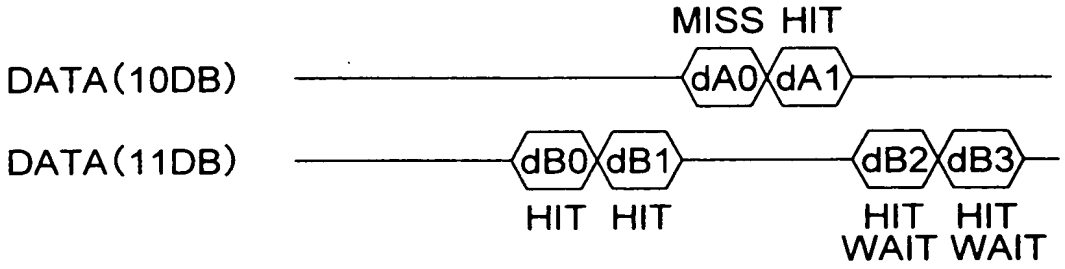


FIG. 19

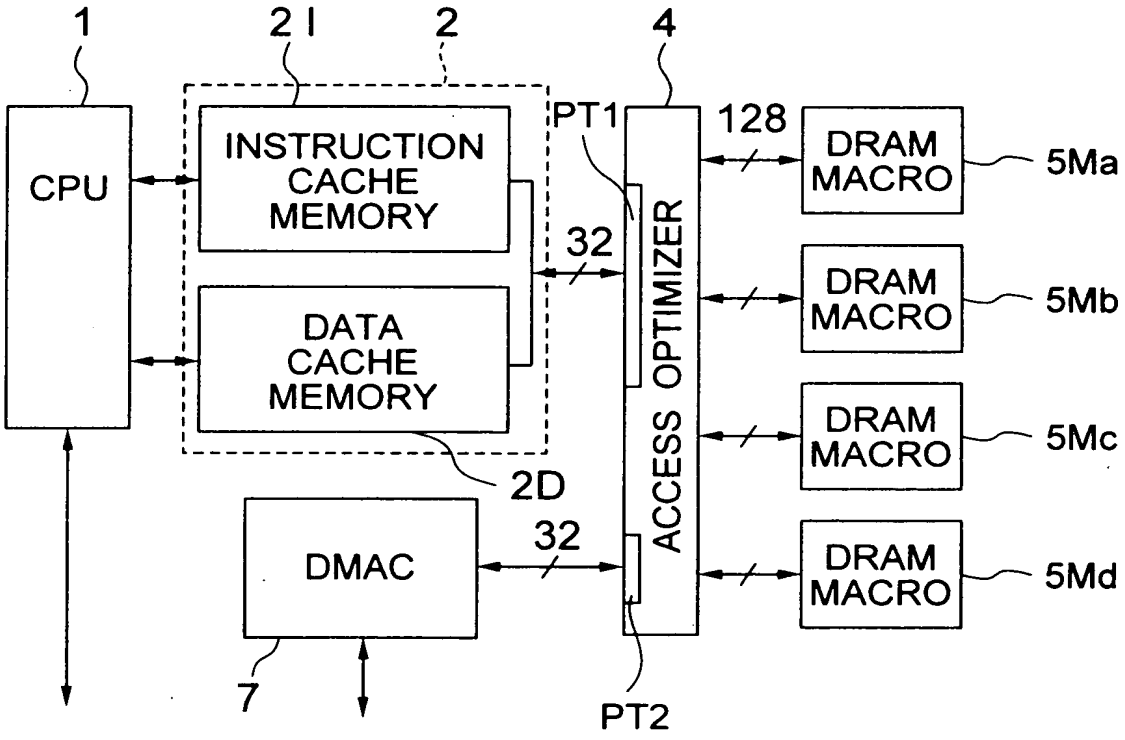

1
21
2
4
CPU
INSTRUCTION CACHE MEMORY
DATA CACHE MEMORY
2D
PT1
32
ACCESS OPTIMIZER
128
DRAM MACRO
5Ma
DRAM MACRO
5Mb
DRAM MACRO
5Mc
DRAM MACRO
5Md
DMAC
32
7
PT2

FIG. 20

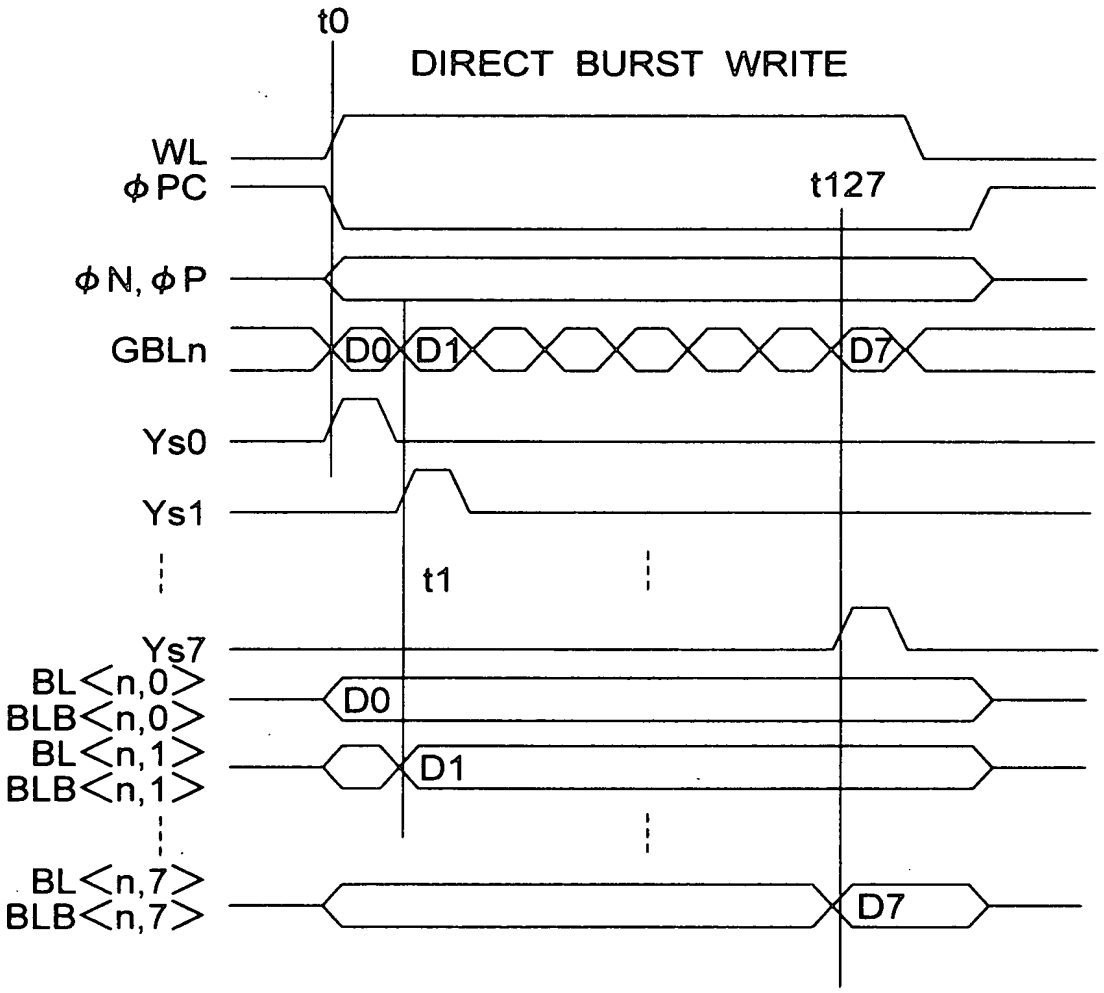

t0
DIRECT BURST WRITE
WL
φPC
t127
φN, φP
GBLn
D0
D1
D7
Ys0
Ys1
t1
Ys7
BL<n,0>
BLB<n,0>
D0
BL<n,1>
BLB<n,1>
D1
BL<n,7>
BLB<n,7>
D7

FIG. 21

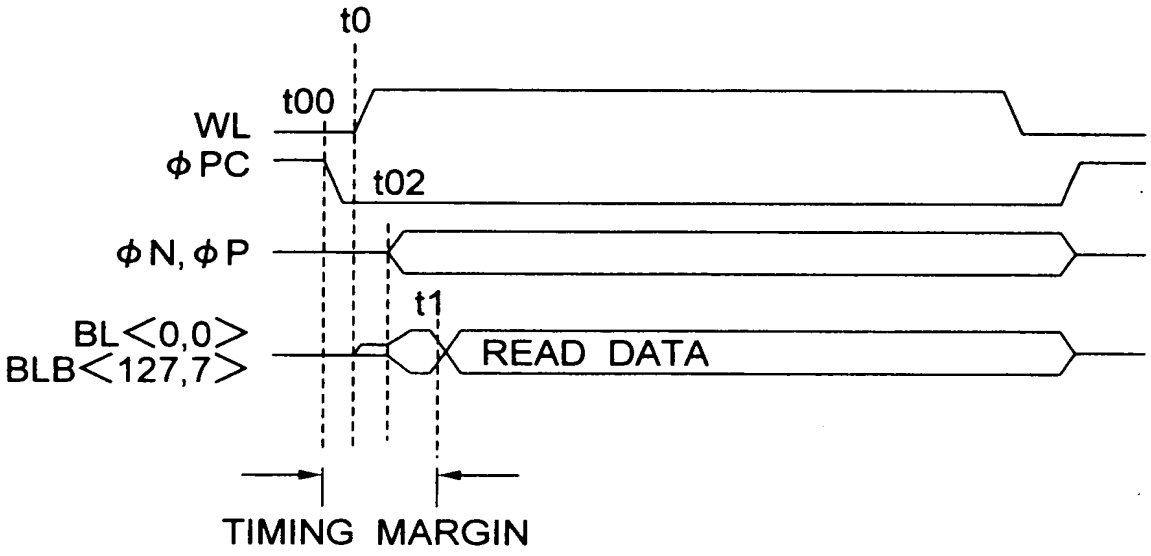
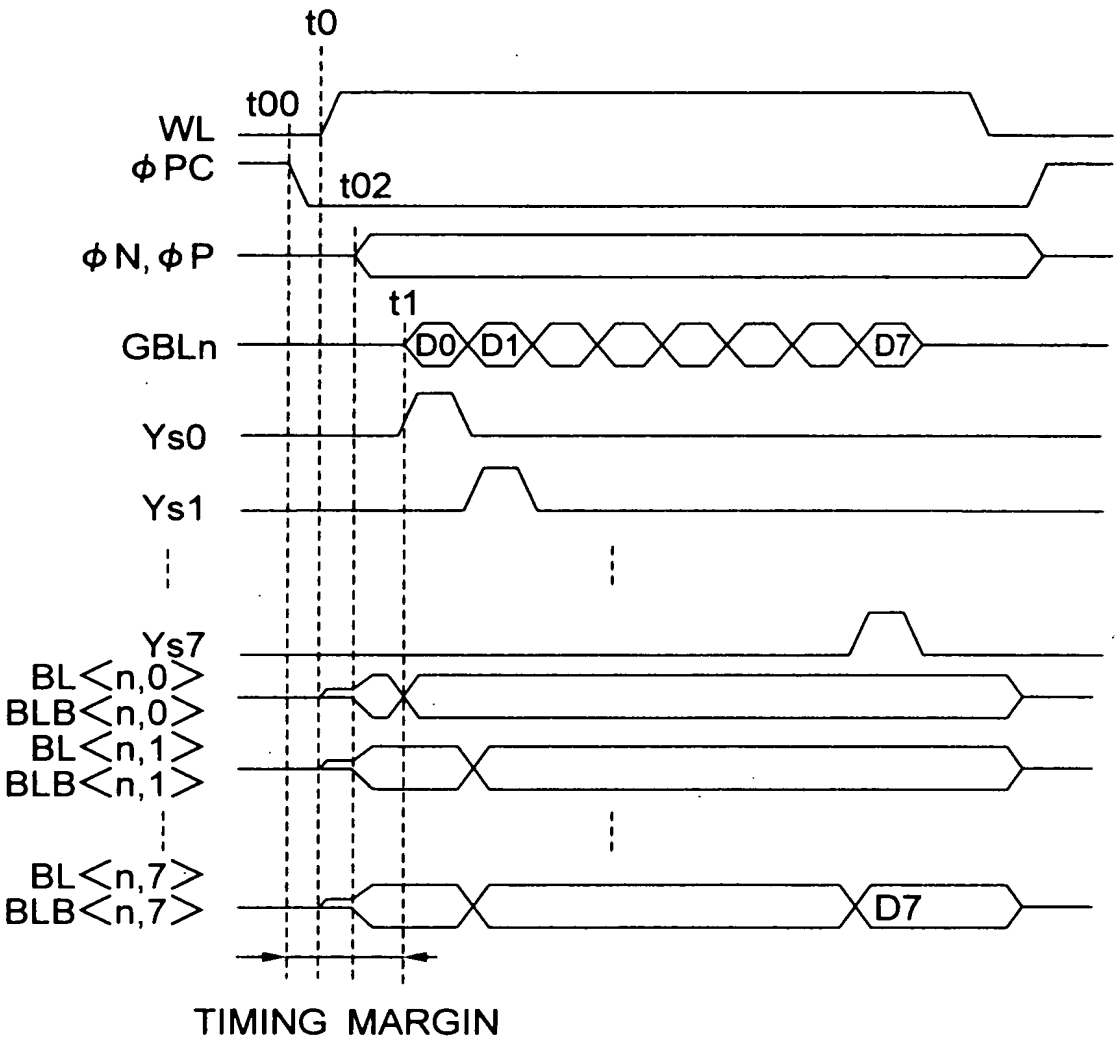

t0
t00
WL
φPC
t02
φN, φP
t1
BL<0,0>
BLB<127,7>
READ DATA
TIMING MARGIN

FIG. 22


t0
t00
WL
φPC
t02
φN, φP
t1
GBLn
D0
D1
D7
Ys0
Ys1
Ys7
BL<n,0>
BLB<n,0>
BL<n,1>
BLB<n,1>
BL<n,7>
BLB<n,7>
D7
TIMING MARGIN